MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Logic Design**			**Module Delivery**	
Module Type	Core			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☒ **Tutorial** ☐ **Practical** ☒ **Seminar**	
Module Code	TU				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Computer science		**College**	CCSM	
Module Leader	Ahmed Saadi Abdullah albasha		**e-mail**	ahmedalbasha@tu.edu.iq	
Module Leader's Acad. Title	Assistant Professor		**Module Leader's Qualification**	master	
Module Tutor	Saif muhaned		**e-mail**		
Peer Reviewer Name	Zaidon Tariq		**e-mail**		
Scientific Committee Approval Date	07/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. To develop problem solving skills and understanding of logic design 2. Teaching students the computer numerical systems 3. Teaching the student the logic gates, their structure, and the truth table 4. Teaching the student the sequential logic circuits, their analysis and installation 5. Teaching students to design and analyze counters and registers and their types 6. Teaching the student the flip flop, its types, the state table and the state diagram
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Knowledge of logic circuits and their design and analysis of complex and synchronous 2. Install logical gates and configure logical circuits 3. Application of logical circuits and their use in random memory 4. Mastering the work of gates and logical circuits and methods of connecting them 5. Knowing ways to connect and deal with half Adder as well as full Adder and how to connect their logical circuits 6. Know how to connect and deal with half Subtract as well as full Subtract and how to connect their logical circuits 7. Know the logical structure of multiplexer and how to connect more than one multiplexer in one logical circuit 8. Knowledge of the logical structure of Flip_Flop of all kinds and how to connect more than one Flip_Flop in one logical circuit
Indicative Contents المحتويات الإرشادية	Indicative content includes the following: <u>Part A – Fundamental concepts</u> Numerical systems and how to convert between them and algebraic and logical operations on them, study logical gates and study how to draw circles and form logical circles from these gates and how to write the expression through drawing [12 hours] <u>Part B- Logic Expressions Simplify, Adder, Subtract</u> The laws of Boolean algebra are studied to simplify Boolean expressions. The K_map method is also studied and applied to simplify Boolean expressions. The addition process is studied based on half Adder and full Adder, in addition to learning the subtraction process based on half subtract and full subtract. [16 hours] <u>Part C- multiplexer ,Decoder</u> A multiplexer, Demultiplaxer and how to connect the function of each of them are

	studied, in addition to how to form multiplexers of large sizes from multiplexers of small sizes. Also, the decoder, encoder and how to connect their logical circuits are understood in detail, in addition to how to connect them together in one circuit. [16 hours] Part D- Flip_flop types ll types of flip-flops are studied and their work is explained in detail and how they work, as well as an explanation of the counter shift register [16 hours)

Learning and Teaching Strategies
استراتيجيات التعلم والتعليم

Strategies	This course is characterized by the fact that it needs a special approach based mainly on the development of engineering thinking and the mathematical approach to thinking. K. Teaching depends mainly on homework that is presented at the end of each week, and the student notes the interdependence between the topics of the series in this course, in addition to assigning the student (or a group of students) to write one report and present it as a seminar for the purpose of training in the use of scientific resources, in addition to Assigning the student with a set of practical experiments that he implements in the laboratory and others that are given as homework, which will help the student to understand more broadly how logical circuits work

Student Workload (SWL)
الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	92	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	4
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	58	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3.8
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1-3 , LO# 9 - 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, LO#8 -10

	Projects	1	10% (10)	Continuous	
	Report	1	10% (10)	12	LO # 5, 9 and 11
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7	LO # 1-8
	Final Exam	2hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction to logic Design and numerical systems
Week 2	Convert between numerical system and mathematical operation on each system
Week 3	Logical gates and how to draw them, and draw logic expression
Week 4	Simplifying Boolean expressions based on the laws of Boolean algebra
Week 5	Simplify Boolean expressions based on K_map (sop) ,(pos)
Week 6	Using full Adder and half Adder in addition
Week 7	Use full subtract and half subtract in subtraction
Week 8	Learn how multiplexers and demultiplexers work and how to connect their logic circuits
Week 9	Learn the work of the decoder and encoder and how to connect their logic circuits
Week 10	Learn about the working of J-K flip flop
Week 11	Learn about the working of J-K flip flop
Week 12	Learn about the working of T flip flop and D flip flop
Week 13	Learn about the working shift Register
Week 14	Learn about the working counters
Week 15	Learn how to draw complex logical circuits consisting of a group of logical circuits that have been studied in previous lectures
Week 16	**Preparatory week before the final exam.**

Delivery Plan (Weekly Lab. Syllabus): There is no Lab activities

المنهاج الاسبوعي للمختبر:

	Material Covered
Week 1	**Lab1_ introduction to Multimedia Logic and crocodile program**
Week 2	**Lab2_ How to draw logical gates and form logical circuits**
Week 3	**Lab3_Simplify logical expressions and draw expressions before and after simplification, noting drawing outputs before and after simplification**

Week 4	**Lab4_Draw circles, half subtract full Adder, Half Adder, full subtract and observe the results of addition and subtraction**
Week 5	**Lab5-Draw multiplexer, demultiplexer, decoder, encoder logic circuits and how to connect them together in one logical circuit**
Week 6	**Lab6-Draw Filp_Flops logic circuits**
Week 7	**Lab7-Dealing with shift register and counter**

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	1. principle of logic design (2020)by (Qasim mohammed Hussein)	Yes
Recommended Texts	Digital logic and computer Design by Morris Mano	No
Websites	Digital Logic And Computer Design By M. Morris Mano (2nd Edition).pdf - Google Drive	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors

	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.